



Description

JMT Dual N-channel Enhancement Mode Power MOSFET

Features

- 30V,22A
 $R_{DS(ON)} < 13m\Omega$ @ $V_{GS} = 10V$
 $R_{DS(ON)} < 19m\Omega$ @ $V_{GS} = 4.5V$
- Advanced Trench Technology
- Provide Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead free product is acquired

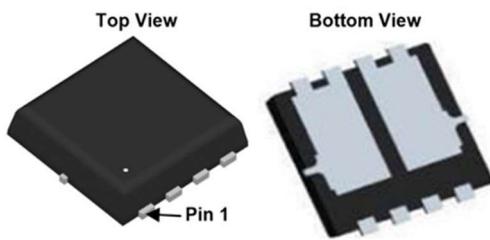
Application

- Load Switch
- PWM Application
- Power management

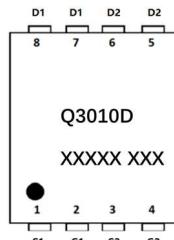


100% UIS TESTED!

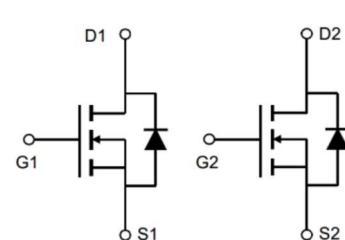
100% ΔV_{ds} TESTED!



PDFN3.3X3.3-8L(Dual)



Marking and pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
Q3010D	JMTQ3010D	TAPING	PDFN3.3X3.3-8L	13inch	5000	50000

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise specified)

Symbol	Parameter		Max.	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current	$T_C = 25^\circ C$	22	A
		$T_C = 100^\circ C$	14	A
I_{DM}	Pulsed Drain Current ^{note1}		88	A
E_{AS}	Single Pulsed Avalanche Energy ^{note2}		24	mJ
P_D	Power Dissipation	$T_C = 25^\circ C$	9.8	W
R_{eJC}	Thermal Resistance, Junction to Case		12.8	$^\circ C/W$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^\circ C$



JMTQ3010D

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=30\text{V}$, $V_{GS}=0\text{V}$,	-	-	1.0	μA
I_{GSS}	Gate to Body Leakage Current	$V_{DS}=0\text{V}$, $V_{GS}= \pm 20\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1.0	1.5	2.5	V
$R_{DS(\text{on})}$ note3	Static Drain-Source on-Resistance	$V_{GS}=10\text{V}$, $I_D=15\text{A}$	-	10	13	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}$, $I_D=10\text{A}$	-	14	19	
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS}=15\text{V}$, $V_{GS}=0\text{V}$, $f=1.0\text{MHz}$	-	1011	-	pF
C_{oss}	Output Capacitance		-	142	-	pF
C_{rss}	Reverse Transfer Capacitance		-	119	-	pF
Q_g	Total Gate Charge	$V_{DS}=15\text{V}$, $I_D=10\text{A}$, $V_{GS}=10\text{V}$	-	19	-	nC
Q_{gs}	Gate-Source Charge		-	6.3	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	4.5	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	$V_{DS}=15\text{V}$, $I_D=20\text{A}$, $R_{\text{GEN}}=3\Omega$, $V_{GS}=10\text{V}$	-	6	-	ns
t_r	Turn-on Rise Time		-	5	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	25	-	ns
t_f	Turn-off Fall Time		-	7	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_s	Maximum Continuous Drain to Source Diode Forward Current	-	-	22	-	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	88	-	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS}=0\text{V}$, $I_s=22\text{A}$	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	$I_F=10\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$	-	7	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	6.3	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: $T_J=25^\circ\text{C}$, $V_{GS}=10\text{V}$, $R_G=25\Omega$, $L=0.5\text{mH}$, $I_{AS}=9.8\text{A}$

3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$

Typical Performance Characteristics

Figure 1: Output Characteristics

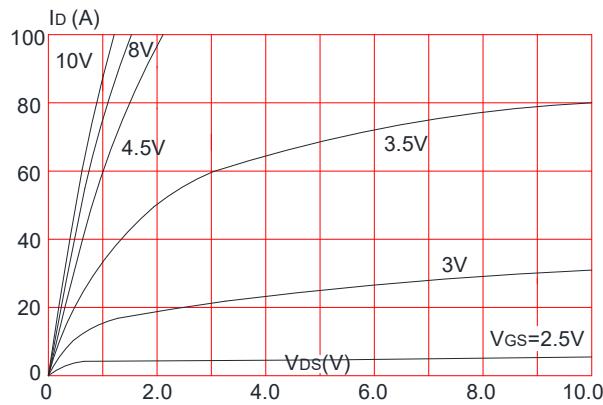


Figure 2: Typical Transfer Characteristics

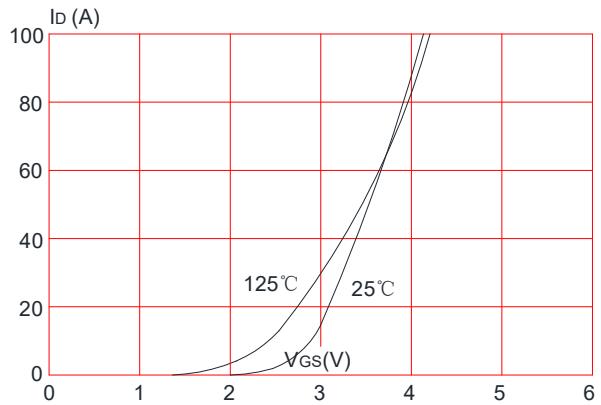


Figure 3: On-resistance vs. Drain Current

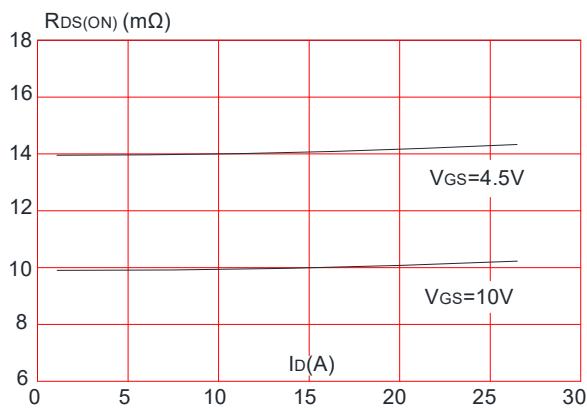


Figure 5: Gate Charge Characteristics

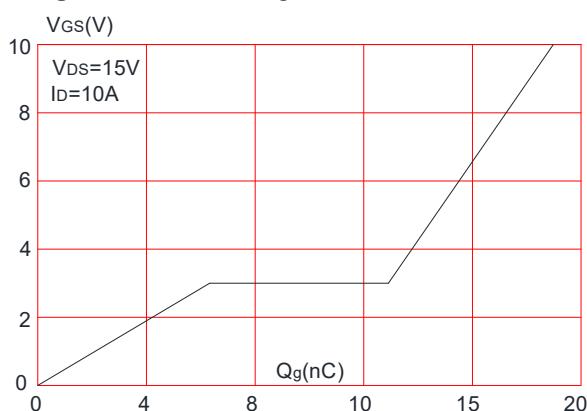


Figure 4: Body Diode Characteristics

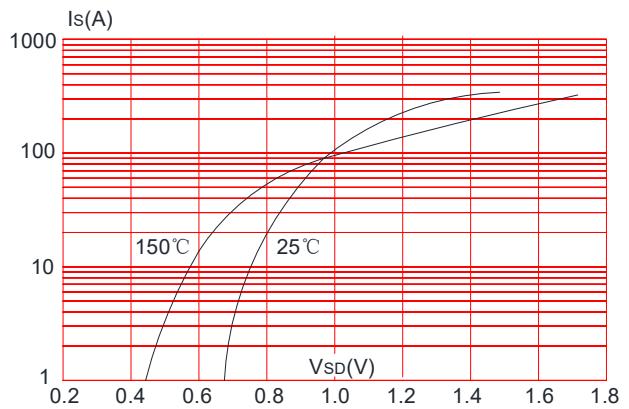


Figure 6: Capacitance Characteristics

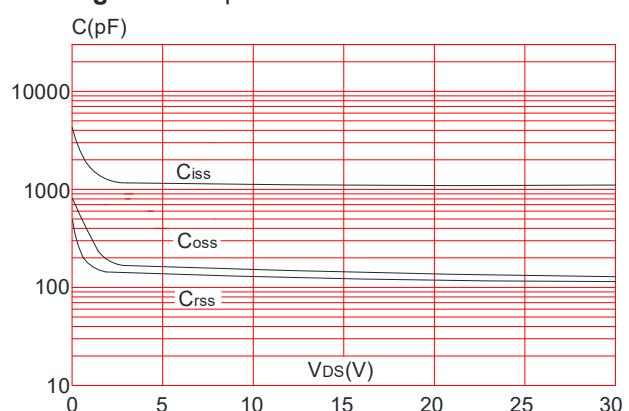


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

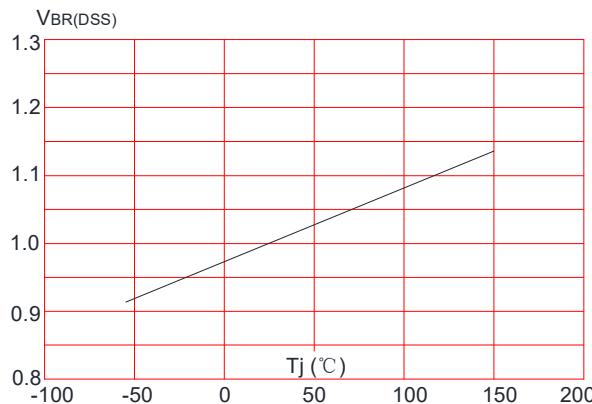


Figure 9: Maximum Safe Operating Area

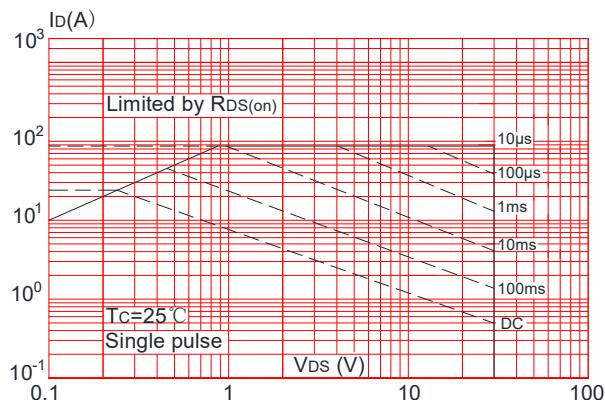


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

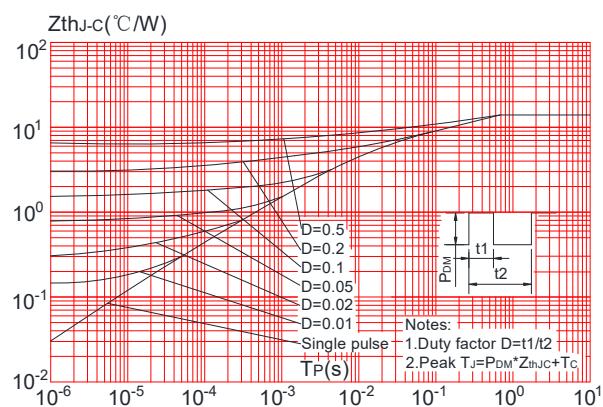


Figure 8: Normalized on Resistance vs. Junction Temperature

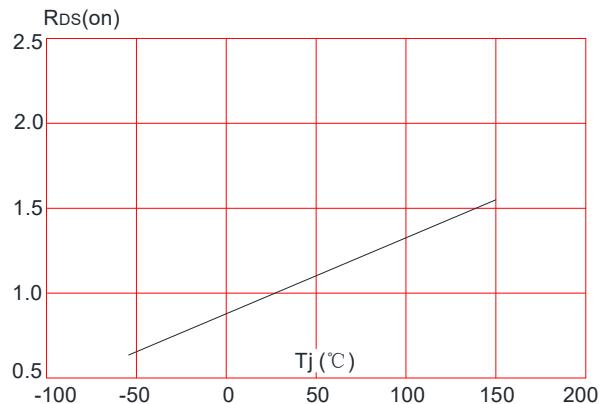
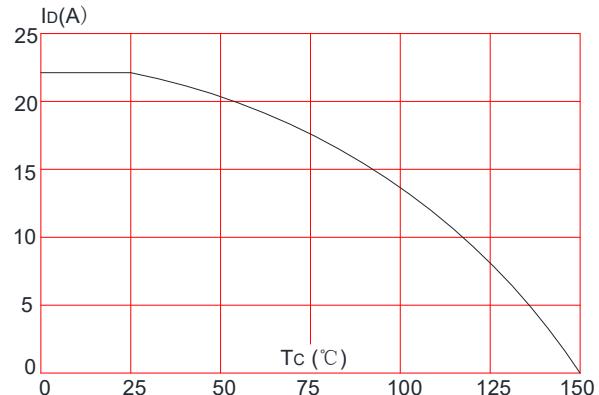


Figure 10: Maximum Continuous Drain Current vs. Case Temperature



Test Circuit

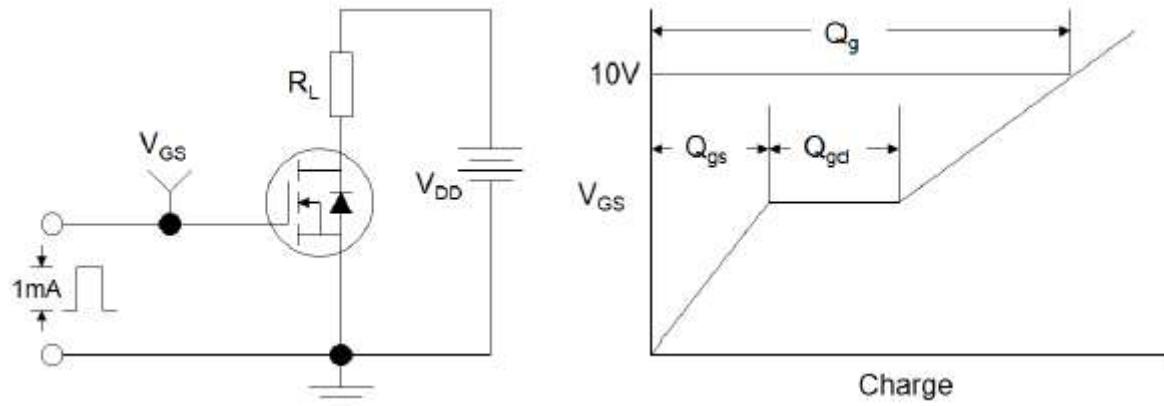


Figure 1: Gate Charge Test Circuit & Waveform



Figure 2: Resistive Switching Test Circuit & Waveforms

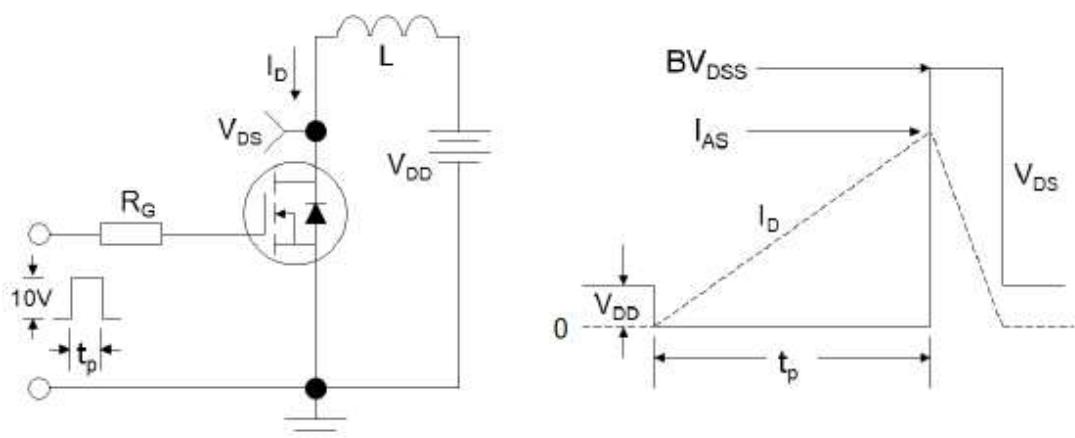
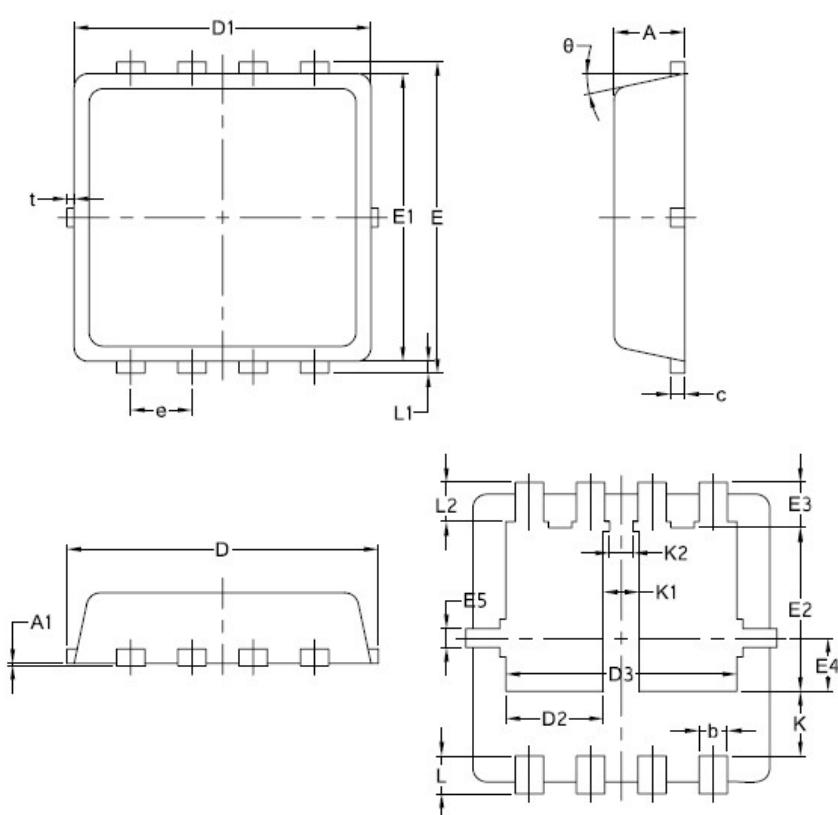


Figure 3: Unclamped Inductive Switching Test Circuit & Waveforms



Package Mechanical Data- PDFN3.3X3.3-8L



SYMBOL	COMMON		
	MM		
	MIN	NOM	MAX
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.25	0.30	0.39
c	0.14	0.152	0.20
D	3.20	3.30	3.45
D1	3.05	3.15	3.25
D2	0.84	1.04	1.24
D3	2.30	2.45	2.60
E	3.20	3.30	3.40
E1	2.95	3.05	3.15
E2	1.60	1.74	1.90
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.50	0.69	0.80
K1	0.30	0.38	0.53
K2	0.15	0.25	0.35
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
L2	0.27	0.42	0.57
t	0	0.075	0.13
theta	10°	12°	14°

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